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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
|---|---|
| RAMSEY, KENNETH J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2879 | |

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/994,511 | Applicant(s) AHN ET AL. | |
|---|---|---|---|
| | Examiner Kenneth J. Ramsey | Art Unit 2879 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *42-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-44,46-78 and 80-84* is/are rejected.

7)☒ Claim(s) *45 and 79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Prior Art Rejections

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 52 - 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (5,458,518) in view of Jones and Aboaf et al (4,016,017). Lee, column 3, lines 43-66, teaches a method of forming a porous dielectric layer in a field emitter display comprising anodizing (etching in hydrofluoric acid solution to which electric power is supplied) a portion of a silicon substrate to form a porous silicon layer and oxidizing at a temperature of 1,000 °C. Lee differs in that there is no disclosure of depositing a poly-silicon layer prior to anodizing. Jones teaches a similar process of forming a dielectric layer in a field emission display and teaches depositing a poly-silicon layer 354 over the cathode column lines 351 prior to treating the poly-silicon to form a porous dielectric layer. It would have been obvious for one of ordinary skill to include a step of forming column lines in the substrate of Lee prior to forming the dielectric layer, since it is well

known to provide addressable field emission sites by such a process. Therefore, to provide a poly-silicon layer on column lines formed on the substrate of Lee prior to forming the dielectric layer by anodizing and oxidizing would have been obvious to one of ordinary skill in the art. As to the amount of porosity of the silicon dioxide, Gnade et al teach forming a porous silicon dioxide layer comprising a silica aerogel (silica is silicon dioxide, see column 7, lines 55-57 and column 8, lines 30-31) having a porosity of between 15-50 percent (column 3, lines 22-23). The preferred higher porosity silicon dioxide has a dielectric constant lower than 2.0, see column 4, lines 1-3 (it is obvious that the higher the porosity, the lower the dielectric constant). Porosity of porous silicon is significantly decreased upon oxidation; note that in Aboaf et al, tables I and II, an initial silicon porosity from 45.6 to 84.7 percent prior to oxidation is required to achieve a porous silicon oxide layer having from 4.5 to 51.7 percent porosity. Therefore, to provide a porosity of greater than 50% porosity before oxidation would have been obvious to one of ordinary skill in the art in the process of Lee et al.

2. Claims 42-44, 46, 49, 50, 56, 59, 60, 62-78 and 80-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Jones as above applied with respect to claim 52 further in view of Gnade et al (5,569,058). Lee differs from claims 42 and 56 in that the field emitters are not formed after the dielectric layer and extraction grid (gate layer) are formed and cavities are etched therein. As shown by Gnade et al, to subsequently deposit emitter material in openings etched in a gate layer and gate insulator is is a well known alternative for forming the emitters. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to form

the emitters 21 of Lee subsequent to the step of forming the dielectric layer and extraction grid, by the process of Gnade et al since it is a well known alternative. As to claims 76-77 and 83-94, Lee taught an oxidizing temperature greater than 1000 °C. As to claims 70 and 75, the columnar nature of anodized porous silicon is well known. As to claims 43 -45, 62-69, 71-74 and 78-82, Gnade et al, column 2, line 60 through column 3, line 30 and column 3, lines 48-54 teach that it was desired to have a high porosity gate insulator in a field emitter display to achieve a low dielectric constant. Further, Gnade et al taught a high porosity silicon dioxide dielectric having a dielectric constant less than 2 (column 5, lines 37-48 and column 8, lines 30-31). It is clearly obvious that the higher porosity silicon dioxide gate insulators have a lower dielectric constant. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have chosen an anodizing time and power sufficient to achieve a high porosity, low dielectric constant gate insulator in Lee as modified by Jones '524 since Gnade et al, column 4, lines 1-3 teach that low dielectric insulators are preferred.

3. Claims 47, 48, 51, 57, 58 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Jones '524, Gnade et al and Aboaf et al as applied to claims 42 and 56 above, and further in view of Jones et al (5,663,608). Lee et al differs from these claims in that a metal doped silicon monoxide field emitter which is coated with a low work function emissive coating is not taught. However, it was known in the art of field emission displays to form a metal doped silicon monoxide emitter which is coated with a low work function emissive material. See Jones et al '608, column 15, lines 27-30 and column 17, lines 8-12. Jones et al '608 indicates that a doped silicon monoxide

emitter is advantageous because it provides a resistive emitter which provides a voltage control for uniform emission from plural emitters (see column 15, line 65 to column 16, line 7). Further, Jones et al '608 teaches that low work function coating is advantageous because of a reduced power requirement (see column 23, lines 63-65). Therefore it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide metal doped silicon monoxide field emitters which may be coated by a low work function material in Lee as modified above in order to obtain uniform field emission with a reduced power requirement. As to claims 48 and 58, Jone et al '608, column 23, lines 48-57 teaches the step of co-depositing the emitter materials and Gnade et al, column 7, lines 23-29 teaches depositing the emitter material at normal incidence to the substrate because a higher aspect ratio of emitter height to base diameter is achieved. Conical emitters are formed by the closing of the opening about the emitter due to stray material buildup (the stray material build up is subsequently removed). With a normal incidence, the holes close up at a slower rate than if the material is deposited at an angle thus forming conical emitters with a higher height to base ratio.

4. s

5. Applicant's arguments filed November 18, 2002 have been fully considered but they are not persuasive. The argument that Gnade et al does not disclose a porous silicon dioxide insulator is not persuasive because silica (silicon dioxide) based materials and silicon dioxide materials would be expected to have essentially the same dielectric constant for a given porosity. Therefore the porosity to obtain the low

dielectric constant specified by Gnade would be relevant to the amount of porosity needed to obtain similar insulator properties in Lee and Jones. The argument that Gnade teaches away form the use of silicon dioxide material as an insulator is taken out of context since the text makes clear that Gnade was speaking only of the "standard" non porous form of silicon dioxide, not the porous form of silicon dioxide employed in Gnade, column 8, lines 30-31. The argument that Lee and Jones teach oppositely from each other and can not be properly combined has no merit as each patent teach the use of porous silicon dioxide as an insulator for a gate electrode and thus are in fact analogous in spite of the different cathode substrates. The differences of these references do not detract from the fact that each in combination with porous silicon dioxide gate insulator have their own advantages as to which there is an obvious choice, and fail to make the teachings thereof non combinable. Rather one of ordinary skill in the art would pick the features thereof that would best meet the purposes intended for the device.

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Action Made Final

1. Applicants' amendments to the claims necessitated the new grounds of rejection herein. Acordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Directions for Responses

Any formal response to this communication should be directed to examiner Kenneth Ramsey, Art Unit 2879, and either
faxed to: 703-872-9319; or mailed to: Box AF
Assistant Commissioner For Patents
Washington, D.C. 20231

Technical inquiries concerning this communication should be directed to Kenneth J. Ramsey, (703) 308-2324 (voice), (703) 746-4832 (fax).

Kenneth J. Ramsey
Primary Examiner
Art Unit 2879